Electric-Field Induced F^- Migration in Self-Aligned InGaAs MOSFETs and Mitigation

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Abstract**—** We report, for the first time, a prominent but fully reversible enhancement in transconductance after applying positive gate stress to self-aligned InGaAs MOSFETs. We attribute this to electric-field-induced migration of fluorine ions (F^-) introduced during the RIE gate recess process. F^- is known to passivate Si donors in InAlAs. In our device structure, an n-InAlAs ledge facilitates the link from the contacts to the intrinsic device. We use secondary ion mass spectroscopy (SIMS) to independently confirm that our process leads to F pile up at the n-InAlAs layer. Transmission line model (TLM) structures confirm F^--induced donor passivation. The understanding derived has lead us to redesign our InGaAs MOSFETs by eliminating n-InAlAs layers and instead use an n-InP ledge. The new device design not only exhibits greatly improved electrical stability but also record performance.

I. Introduction

InGaAs has emerged as a promising n-channel material candidate for future nano-scale CMOS thanks to its low operating voltage and superior electron transport properties [1]. Recently, self-aligned InGaAs Quantum-Well (QW) MOSFETs have achieved record performance [2] and impressive FinFETs have also been demonstrated [3]. As device technology continues to improve, attention is turning to the electrical reliability of this device family.

In InGaAs MOSFETs, there have been multiple reports of positive threshold voltage (V_t) shifts coupled with trans-conductance (g_m) degradation following positive gate voltage stress. This is known as Positive Bias Temperature Instability (PBTI) [4,5,6]. Here, we report an anomalous g_m *enhancement* in self-aligned InGaAs MOSFETs under PBTI conditions that is fully reversible. We attribute this to F^- migration and Si-donor passivation/depassivation in n-InAlAs used in the link region between the intrinsic and extrinsic portions of the device. As F-based RIE and chemical treatments are important in device fabrication, understanding and mitigating the effects of F contamination on performance and reliability are crucial for the adoption of InGaAs MOSFETs for future CMOS. Our diagnosis of this problem has led us to an alternative device design that mitigates instability and yields record performance.

II. Anomalous Voltage Stress Behavior

The studied QW InGaAs MOSFETs have a cross section depicted in Fig. 1. The heterostructure is grown by MBE and comprises a composite n^+ cap of n-InGaAs/n-InP/n-InAlAs/i-InP, an intrinsic channel of $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ (3/2/5 nm) and a buffer of InAlAs on an InP substrate. Si is the dopant in all n-type layers. Devices were fabricated by a contact-first, gate-last process [7]. Mo/W ohmic contact was first sputtered and defined by F-based RIE. To achieve self-aligned gate and contacts, the cap was subsequently recessed by a combination of Cl-based RIE and digital etch. The device was then thermally annealed at 340°C for 15 min to repair RIE damage. The gate stack consists of 2.5 nm HfO_2 deposited by ALD at 250°C and E-beam evaporated Mo. The final channel thickness is 7 nm.

We have studied the stability of devices with 85 nm long access region. Shorter ledge devices behave similarly. We first performed forward gate stress experiments, in which a positive gate overdrive voltage was applied ($V_{gt}=V_{gs}-V_t>0$, $V_{ds}=0$ V) followed by device recovery with all terminals grounded. I-Vs were measured periodically to map the device evolution. We monitor linear threshold voltage, V_{tlin} (defined at 1 μA/μm, $V_{ds}=0.05$ V), peak transconductance, $g_{m,max}$ (at $V_{ds}=0.5$ V), minimum subthreshold swing, S_{min} (at $V_{ds}=50$ mV), and ON-resistance R_{on} (at $V_{gt}>0.6$ V, $V_{ds}=0.05$ V). A final 20 min, 70°C thermal step was used to assess any permanent degradation.

Fig. 2 shows the evolution of g_m characteristics of a typical device during stress at $V_{gt}=0.8$ V for 1.5 h and subsequent recovery, all at room temperature (RT). During stress, V_t shifts positively, similar to what is observed in PBTI experiments due to oxide trapping [4,5,6]. In contrast, there is a remarkable *increase* in $g_{m,max}$ of as much as 50%. During the following 2-h recovery, g_m and V_t recover near completely. Throughout the experiment, S_{min} changes negligibly (not shown).

Fig. 3 shows the impact of different gate overdrive stress voltage on $g_{m,max}$, V_{tlin}, and R_{on}. For moderate stress time ($<10^3$ sec), $g_{m,max}$ increases, V_t shifts positively and R_{on} decreases. All changes are enhanced by stress voltage. After prolonged stress time ($>10^3$ sec) at high stress voltage ($V_{gt}=1$ V), $g_{m,max}$ and R_{on} start to degrade due to a separate mechanism. Fig. 4 shows that $\Delta g_{max}/g_{max0}$ and $\Delta R_{on}/R_{on0}$ are inversely correlated under all but the harshest stress conditions. In contrast, there is no relation between $\Delta g_{max}/g_{max0}$ and ΔV_{tlin} (not shown), indicating that PBTI alone cannot explain our observations.

We have also performed OFF-state stress experiments with high V_{ds}. I-V characteristics were collected in the normal mode and after swapping source and drain. Fig. 5 shows g_m evolution during stress at $V_{gt}=0$ V and $V_{ds}=0.7$ V for 2 h at RT. As stress time increases, in the normal configuration, V_t shifts negatively and g_m increases (Fig. 5a). With source and drain reversed, the V_t shift is still negative but g_m degrades (Fig. 5b). The changes in g_m are consistent with a reduction in access resistance on the source side but an increase on the drain side.

Our experiments suggest a strong connection between g_m instability and the extrinsic portion of the device, inexplicable by established PBTI phenomena. We postulate mobile F^- to be

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the cause. F is introduced during Mo contact etching by SF_6/O_2 RIE. This defines the intrinsic device and, hence, we expect F^- to concentrate under the gate and in the access regions, which consist of a Si-doped InAlAs ledge. F^- is known to reversibly passivate Si in n-InAlAs (but not n-InP or n-InGaAs) [8,9]. F^- bound to Si in InAlAs can easily dissociate and migrate under an electric field [10]. Under forward gate stress $V_{gt} > 0$, F^- drifts from the access regions into the gate oxide (Fig. 6a). This reactivates the Si dopants in the n-InAlAs ledge, enhancing the sheet electron concentration in the access region and reducing its resistance. The presence of F^- ions in the oxide shifts V_t positively, adding to the positive V_t shift expected from PBTI. Under OFF-state $V_{ds} > 0$ stress, the lateral E-field sweeps F^- away from the source and gate oxide towards the drain. This reduces R_s and increases R_d, thus improving g_m in the forward mode but degrading it in the reverse mode (Fig. 6b). Both configurations show a negative V_t shift as F^- exits the oxide.

III. Independent Verification of Fluorine

To verify our hypothesis, we performed SIMS on three samples with heterostructure containing a 3 nm-thick n-InAlAs layer. Sample A was never exposed to F. Sample B was exposed to Mo sputtering and F-based RIE. Sample C was further annealed at 350°C for 1 min. Compared to A, samples B and C show a high surface concentration of F (Fig. 7). Sample C shows an additional pile-up of F in the n-InAlAs layer that integrates to a concentration of 5.3×10^{14} cm^{-2} (much of it likely in the neutral form). This is much higher than in earlier studies in HEMTs where F was introduced through HF treatments [8, 9], instead of F-RIE, as done here. SIMS also shows that F does not reach the Si δ-doped layer beneath the channel. From these results, we expect a similar F pile up in the n-InAlAs layer of the MOSFET access region (Fig. 1).

To verify F^- induced donor passivation, we fabricated two types of TLMs on a sample with an n-InGaAs/n-InP/n-InAlAs (15/3/3 nm) cap. The first type used sputtered Mo contacts etched by SF_6/O_2 RIE (as in the MOSFET process). The second type used lift-off Mo contacts, and hence had no exposure to F. Both TLMs were measured before and after annealing at 350°C for 1 min (Fig. 8). Before annealing, the F-RIE sample exhibits a semiconductor sheet resistance (R_{sh}) of 176 Ω/□, 30% higher than that of the lift-off sample. After annealing, R_{sh} of the lift-off sample decreased somehow, while R_{sh} of the F RIE sample increased by 3x. This result is consistent with literature findings that a thermal step is needed for F to migrate to Si-doped InAlAs and passivate the Si donors [8-10].

IV. Alternative MOSFET Design

With F a key element in semiconductor manufacturing, mitigation of F-dopant passivation necessitates the elimination of n-InAlAs from the device structure. Despite its wide use in InGaAs FETs, this material is not essential. We have designed and fabricated an alternative MOSFET structure that instead uses n-InP in the access region (Fig. 9). The original (sample "1") and the alternative (sample "2") designs share the same intrinsic channel and gate stack. The immunity of the new n^+ ledge to F passivation results in virgin devices from sample "2" with a higher electron concentration in the access regions than in sample "1". This has led to a record low ON-resistance and high transconductance of $g_{m,max}$ = 3.45 mS/μm [2], the highest among InGaAs FETs of any kind (Fig. 10). More significantly, the new device structure is far more stable.

We have repeated the stress experiments on sample "2" and compared results with sample "1". Under forward gate stress, the new design shows a $g_{m,max}$ decrease (up to 15%) and a small positive V_t shift (Fig. 11) that are largely recoverable after thermal detrapping. This is classic PBTI behavior attributed to electron trapping in the oxide. Fig. 12 shows the impact of gate overdrive stress voltage on the time evolution of $g_{m,max}$, R_{on} and V_{tlin}. g_m degradation and V_t shifts are enhanced by stress voltage and time. ΔV_{tlin} is generally smaller in sample "2", reflecting the absence of F in the ledge next to the gate stack. Fig. 13 confirms classical PBTI behavior in sample "2", where $\Delta g_{max}/g_{max0}$ strongly correlates with ΔV_{tlin} at all $V_{gt,stress}$. This is consistent with charge trapping near the III-V/high-k interface [4,5]. The correlation between ΔV_{tlin} after 2-h stress at different $V_{gt,stress}$ and ΔV_{tlin} after 1.5-h recovery shows a trend observed in other PBTI studies [4]. Unlike sample "1", changes in g_m and R_{on} are uncorrelated in sample "2". In fact, under moderate stress, R_{on} changes minimally, in contrast with sample "1" (Fig. 3). However, after prolonged harsh stress, R_{on} degrades, perhaps by a different mechanism also observed in sample "1". Under OFF-state stress (Fig. 14) sample "2" shows minimal changes. Thus, by substituting n-InAlAs with n-InP, we have greatly improved the device electrical stability, while substantially gaining in device performance.

V. Temperature Dependence of F^- Donor Passivation vs. Oxide Trapping

Studying the temperature (T) dependence of degradation under stress on both samples yields further insight into the relevant physics. Figs. 15 and 16 compare the T dependence of g_m and R_{on} in samples "1" and "2". Sample "2" shows a weakly T-activated degradation in g_m, with minimal change in R_{sd} at all T. In contrast, sample "1" shows strong T-enhancement of g_m increase and R_{on} reduction during stress, and prominent recovery after resting at the same stress T. This reflects T-enhanced F^- migration characterized by an E_A=0.23±0.05 eV (Fig. 17), attributed to F-Si ionization energy [11].

Fig. 18 compares the T dependence of ΔV_{tlin} in both samples during stress. Sample "2" shows a weak T dependence with E_A=0.062±0.004 eV (Fig. 19), slightly lower than what others have reported: 0.08-0.13 eV [5,6]. This is likely due to the QW nature of our device design that reduces the defect barrier offset [5]. In contrast, the T-enhanced V_t shift in sample "1" reflects the additive nature of oxide trapping and F migration into the oxide. Both samples exhibit mild S degradation (<20 mV/dec) that is T-activated (not shown), commonly observed in PBTI experiments [12].

VI. Conclusions

We have identified a new instability mechanism in self-aligned InGaAs MOSFETs caused by F^- migration and (de)-passivation of Si dopants in n-InAlAs. Positive gate voltage stress leads to reversible g_m enhancement, contrary to well established PBTI phenomena. We have successfully mitigated this problem by eliminating n-InAlAs from the device structure. The new device design not only shows improved stability, but also achieves record device performance.

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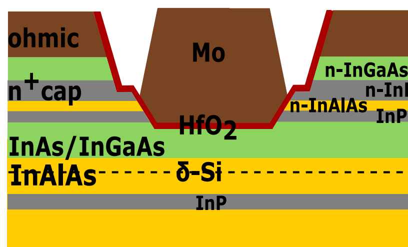

Fig. 1. Cross sectional schematic of self-aligned InGaAs MOSFETs used in this study. Unless indicated, layers are undoped (sample "1").

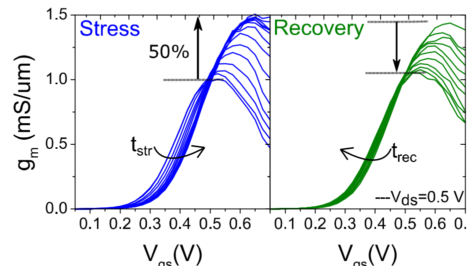

Fig. 2. Evolution of g_m characteristics (left) during gate stress at V_{gt}=0.8 V and V_{ds}=0 V for 1.5 h, and (right) during recovery at RT. L_g=200 nm (sample "1").

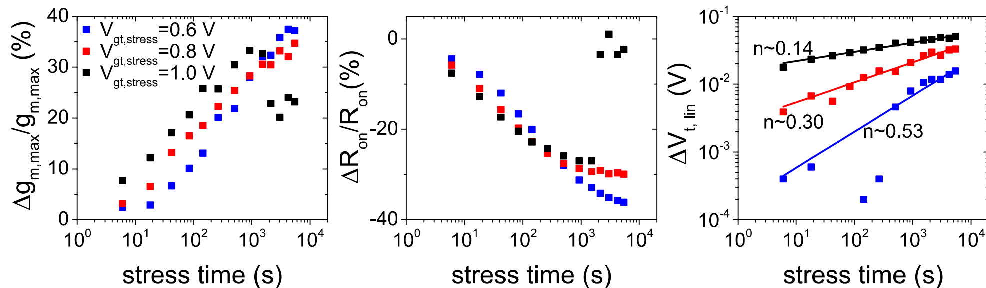

Fig. 3. From left to right: evolution of g_{max}, R_{on} and V_{tlin} during 2-h positive gate voltage stress at different V_{gt} with V_{ds}=0 V at RT. The fits to V_{tlin} represent a saturating power law characteristic of PBTI with the indicated time exponent n (sample "1").

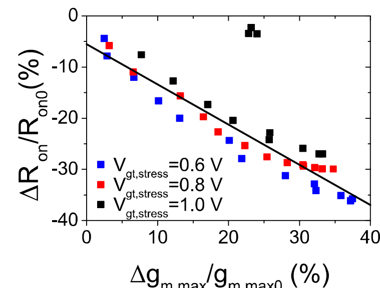

Fig. 4. Correlation between $\Delta R_{on}/R_{on0}$ and $\Delta g_{max}/g_{max0}$ at different $V_{gt,stress}$ for the experiment of Fig. 3 (sample "1").

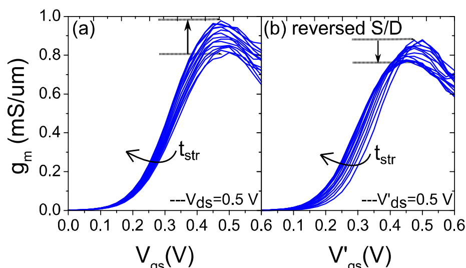

Fig. 5. Evolution of g_m characteristics during OFF-state stress for 2 h at RT under V_{gt}=0 V, V_{ds}=0.7 V: (a) measured in normal configuration, and (b) with source and drain terminals reversed (sample "1").

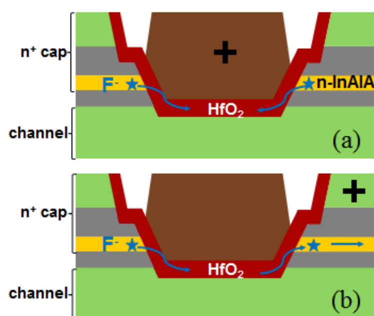

Fig. 6. Illustration of fluorine ion migration due to (a) forward gate bias with V_{gt}>0 and (b) OFF-state bias with V_{ds}>0.

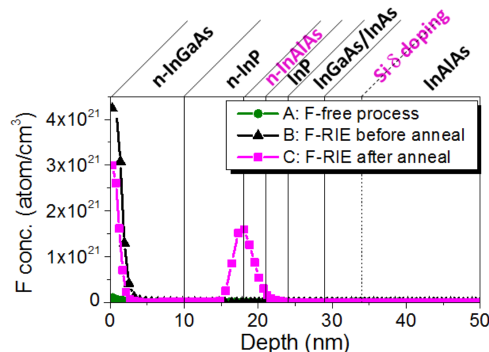

Fig. 7. Fluorine concentration versus depth from SIMS for samples A (never exposed to F), B (F-based RIE) and C (F-based RIE + 350°C anneal for 1 min). The layers are labeled on the top. A prominent F peak in the Si-doped InAlAs layer is observed in sample C.

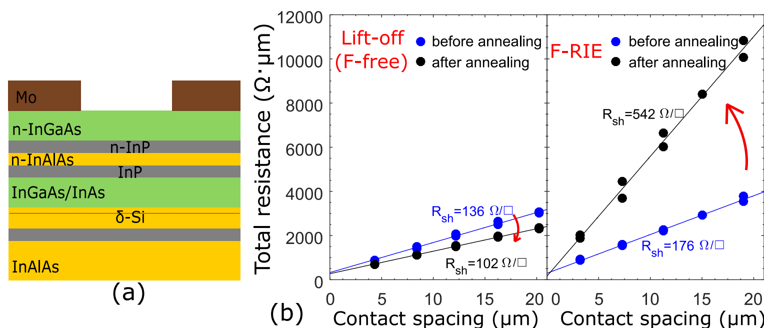

Fig. 8. (a) Schematic of TLM structure. (b) TLM resistance versus contact distance before and after annealing on (left) samples fabricated by lift-off (no F exposure), and (right) samples that have undergone F-based RIE.

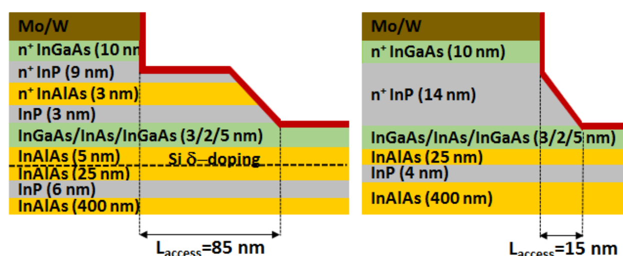

Fig. 9. Design of the original (sample "1") used earlier in this paper and alternative (sample "2") device structure. InAlAs layers in Sample 2 are undoped.

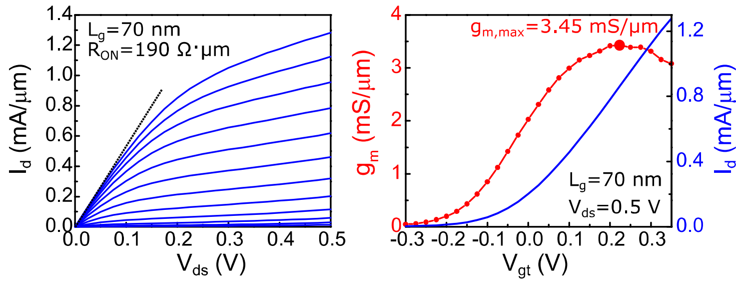

Fig. 10. L_g=70 nm InGaAs MOSFET from sample "2": (a) output I_d-V_{ds} with V_{gt} =-0.2 to 0.35 V in 0.05 V steps and (b) g_m and transfer characteristics at V_{ds}=0.5 V. $g_{m,max}$=3.45 mS/μm represents a record among InGaAs FETs [2].

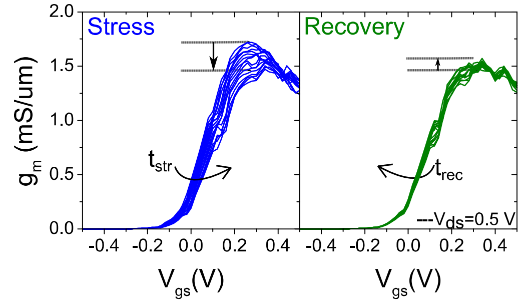

Fig. 11. Sample "2": evolution of g_m characteristics (left) during gate stress at V_{gt}=0.8 V and V_{ds}=0 V for 2 h and (right) during 1.5-h recovery at RT.

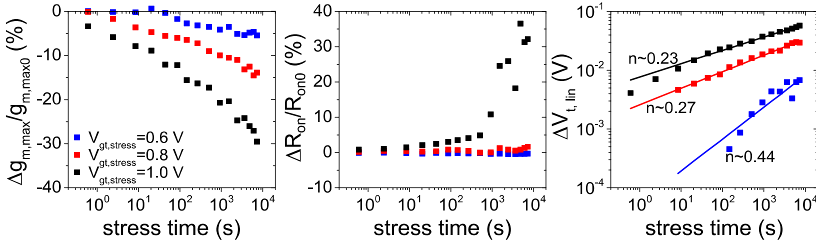

Fig. 12. Sample "2": evolution of g_{max}, R_{on} and V_{tlin} during 2-h positive gate voltage stress at different V_{gt} with V_{ds}=0 V at RT. The fits to V_{tlin} represent a saturating power law characteristic of PBTI with the indicated time exponent n.

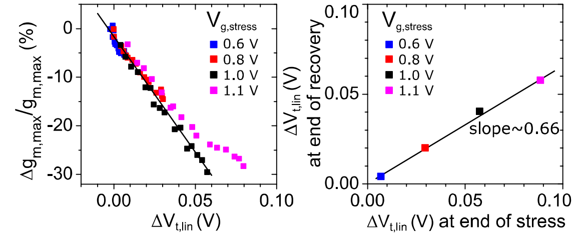

Fig. 13. Sample "2" shows classical PBTI behavior: (left) strong correlation between $\Delta g_{max}/g_{max0}$ and ΔV_{tlin} at different $V_{gt,stress}$ and (right) trend of ΔV_{tlin} after 1.5-h recovery vs ΔV_{tlin} after 2-h stress at different $V_{gt,stress}$, similar to other PBTI studies [4, 5, 6].

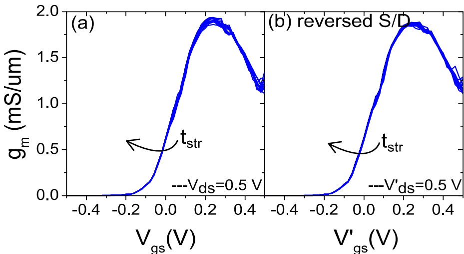

Fig. 14. Sample "2": evolution of g_m characteristics during OFF-state stress for 2 h at RT under V_{gt}=0 V, V_{ds}=0.7 V stress, (a) measured in normal configuration, and (b) with source and drain terminals reversed.

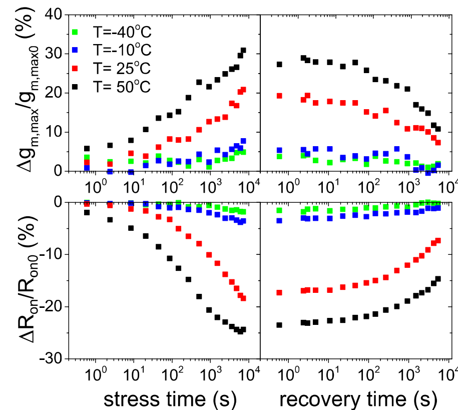

Fig. 15. Sample "1": evolution of g_{max} and R_{on} during 2-h positive gate voltage stress at different stress temperatures (T=-40°C, -10°C, 25°C, 50°C) with V_{gt} =0.8 V, V_{ds}=0 V, and during subsequent 1.5-h recovery at the same temperatures.

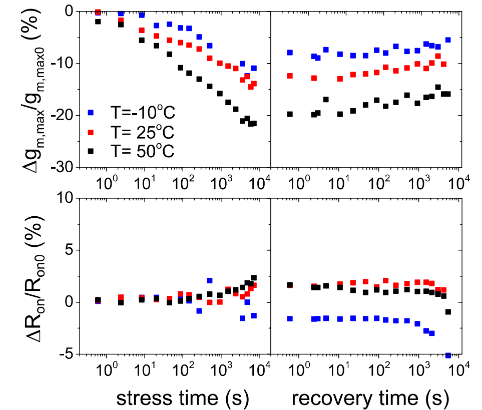

Fig. 16. Sample "2": evolution of g_{max} and R_{on} during 2-h positive gate voltage stress at different stress temperatures (T=-10°C, 25°C, 50°C) with V_{gt} =0.8 V, V_{ds}=0 V, and during subsequent 1.5-h recovery at the same temperatures.

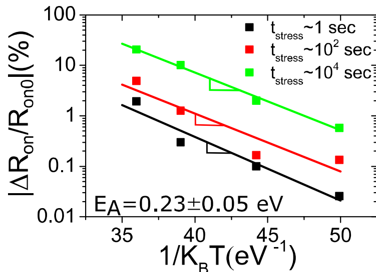

Fig. 17. Sample "1": Arrhenius plot of $\Delta R_{on}/R_{on0}$ measured during stress. Activation energy E_A is extracted to be 0.23±0.05 eV.

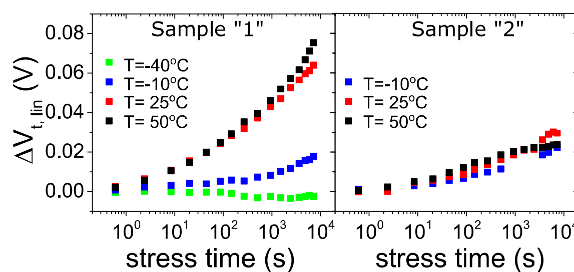

Fig. 18. Comparison of temperature dependence in ΔV_{tlin} evolution during 2-h positive gate voltage stress (V_{gt} =0.8 V, V_{ds}=0 V) at different stress temperatures between (left) sample "1" and (right) sample "2".

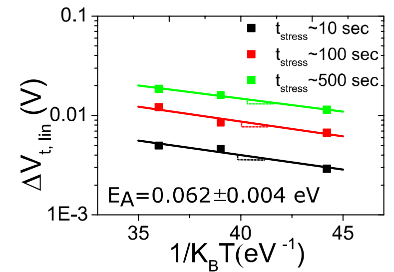

Fig. 19. Sample "2": Arrhenius plot of ΔV_{tlin} measured during stress. Activation energy E_A is extracted to be 0.062±0.004 eV.